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India Semiconductor Mission

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India Semiconductor Mission

India’s chip programme is moving from its first phase to its second. Semicon 2.0 was approved in July 2026. This lesson covers its pillars, the first phase, the plants, a new silicon carbide unit, chip design and talent.

The idea in brief

- **Jul 2026** Semicon 2.0 approved
- **Rs 1,27,500 cr** Semicon 2.0 outlay
- **12** Units approved in ISM 1.0
- **2028** First fab due

The Programme

Semicon 2.0 Basics

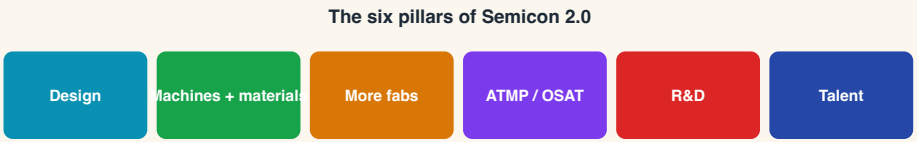
What is Semicon 2.0?

Semicon 2.0 is the second phase of India’s chip programme. The Union Cabinet approved it in **July 2026**. The total outlay is **Rs 1,27,500 crore**.

Think of it as the next big step after the first phase. The first phase built the base. The second phase aims to fill the gaps.

What are its six pillars?

The programme aims to build the chip ecosystem as a whole. It rests on **six pillars**.



Six pillars, one ecosystem.

The six pillars

Pillar	What it covers
Design	Chip design startups and tools
Machines and materials	Equipment and inputs for plants
More fabs	Wafer fabrication units
ATMP / OSAT	Assembly, testing and packaging
R&D	Research and development
Talent	Trained engineers and technicians

The design pillar comes first in the official list.

Think it through: How do I remember the pillars?

Walk along the chip's journey. First it is designed. Then machines and materials are needed. Then fabs make it, packaging finishes it, research improves it, and talent runs it all.

Quick check 1. True or false: Semicon 2.0 has a total outlay of Rs 1,27,500 crore. *(True or False?)* See answer ↓

Quick check 2. True or false: Semicon 2.0 rests on four pillars. *(True or False?)* See answer ↓

Sources: pib.gov.in

The First Phase

What was the first phase?

The first phase is called **Semicon 1.0** or ISM 1.0. Its outlay was **Rs 76,000 crore**. The India Semiconductor Mission (ISM) acts as the nodal agency.

ISM 1.0 was planned as a **six-year programme**. It achieved its objectives in just four years.

How does the Fabs scheme help a company?

A company that builds a fab gets fiscal support of **50% of the project cost**. This is given on a pari-passu basis. The support period is six years.

Pari-passu means both sides put in money together, on equal terms. The state does not pay first and then wait.

Which kind of fab qualifies?

The scheme backs a **Silicon CMOS based fab**. It can make logic, memory, digital, analog and mixed-signal chips. It can also make systems on a chip.

ISM 1.0 against Semicon 2.0

Item	ISM 1.0	Semicon 2.0
Outlay	Rs 76,000 crore	Rs 1,27,500 crore
Planned length	Six years	Six pillars
Fab support	50% of project cost	Part of the pillar on more fabs

Rows are not strict opposites. Read each cell alone.

What is the scheme's larger goal?

The scheme aims to attract large investments in wafer fabrication. It also wants to build a **trusted value chain**. That helps the wider electronics ecosystem.

> **Think it through:** Why mention pari-passu?
>
> It is a favourite word for exam writers. The Fabs scheme shares cost equally. The government's equity share will not exceed 49% of the total project equity.

> **Quick check 3.** True or false: ISM 1.0 was planned as a six-year programme. *(True or False?)* See answer ↓

> **Quick check 4.** True or false: The Fabs scheme gives support of 25% of project cost. *(True or False?)* See answer ↓

Sources: ism.gov.in; pib.gov.in

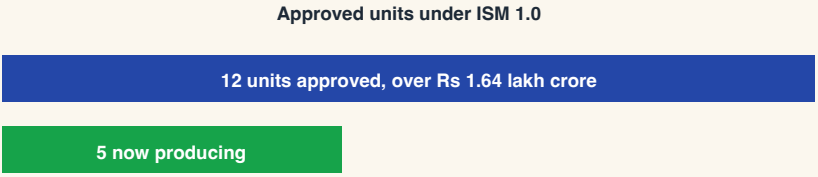
Plants and Units

Plants and Fabs

How many units were approved?

Twelve manufacturing units were approved under ISM 1.0. The cumulative investment is over **Rs 1.64 lakh crore**.

The list has one silicon fab, one silicon carbide fab and one GaN micro LED display fab. It also has nine packaging units.



Twelve approved, five producing. Bars are not to scale.

How many plants are producing now?

Five plants have started commercial production. Their chips are being exported in addition to meeting domestic needs.

Three companies are named: **Micron, Kaynes and CG Semi**. They have started commercial production.

When will the first fab arrive?

The first fab is scheduled to be commissioned in **2028**. A fab due in 2028 already has a large part of its capacity booked.

A fab is a plant that makes chips on silicon wafers. The plants running today do assembly and packaging, which come after that step.

> **Think it through:** Is the first fab already running?
>
> No. The date to remember is 2028. Do not confuse the packaging plants that already ship chips with the fab that is still to come.

> **Quick check 5.** True or false: Twelve manufacturing units have been approved under ISM 1.0. *(True or False?)* See answer ↓

> **Quick check 6.** True or false: The first fab is scheduled to be commissioned in 2026. *(True or False?)* See answer ↓

Sources: pib.gov.in

The SiCSem Unit

What did the Unit Approval Committee clear?

The 217th meeting of the Unit Approval Committee (UAC) approved the proposal of **SiCSem Private Limited**. It is a semiconductor manufacturing unit. The location is in **Khordha district, Odisha**.

What will the unit make?

It will make **Silicon Carbide (SiC)** devices, including SiC diodes and SiC MOSFETs. The site spreads over **21.889 acres**.

SiC is a tough material that handles heat and high voltage well. That is why it is used in power devices.

SiCSem at a glance

Item	Figure
Investment	Rs 3,406 crore
Jobs	About 1,270
Diodes a year	4.8 million
MOSFETs a year	91.2 million
Site	21.889 acres

Numbers come from the PIB release of 15 September 2026.

Why does this unit matter?

It is the second silicon carbide unit approved in Odisha. The investment is **Rs 3,406 crore**. The project is expected to create about **1,270 jobs**.

Think it through: How do I keep the numbers straight?

Remember 4.8 million diodes and 91.2 million MOSFETs. Diodes are fewer. MOSFETs are far more.

Quick check 7. True or false: SiCSem will make SiC diodes and MOSFETs. *(True or False?)* See answer ↓

Quick check 8. True or false: The SiCSem investment is Rs 3,406 crore. *(True or False?)* See answer ↓

Sources: pib.gov.in

People and Chips

The Design Pillar

Why does the design pillar come first?

Design means planning a chip before it is made. The PIB release says chip design contributes up to **50% of overall value addition**. It accounts for about **15-35% of the bill of materials** cost of electronic products.

So a country that designs chips keeps a large share of the value. This is the logic behind the first pillar.

How many startups are designing chips?

There are **105 startups** already developing chips. The design tools reached **455 organisations**. These include 350 academic institutions and 105 startups.

What support do design projects get?

Twenty-four design projects from startups and MSMEs have been approved for financial support. And 105 startups and MSMEs got access to design tools (EDA tools).

EDA stands for Electronic Design Automation. These are software tools used to design chips.

The design ecosystem

Item	Number
Startups developing chips	105
Design projects approved	24
Organisations given design tools	455
Academic institutions among them	350

All numbers are from PIB releases of July and August 2026.

What is the VIHAAN chip?

Aheesa Digital Innovations achieved first-pass silicon success with **VIHAAN**. It is a broadband chip built on the indigenous **VEGA microprocessor**. The company now heads towards production tape-out, targeted for **2027**.

Where are such chips used?

Chips designed under the scheme serve satellite communications, drones, surveillance cameras and Internet of Things devices. They also serve LED drivers, AI systems, telecom equipment and smart meters.

> **Think it through:** Why is ‘first-pass success’ a big deal?
>
> A chip design can fail on its first try, which wastes time and money. Getting it right the first time shows the design was strong.

> **Quick check 9.** True or false: Aheesa's VIHAAN chip is built on the indigenous VEGA microprocessor. *(True or False?)* See answer ↓

> **Quick check 10.** True or false: Design tools reached 455 organisations, including 350 academic institutions. *(True or False?)*
>
> See answer ↓

Sources: pib.gov.in; ism.gov.in

Talent and Skills

How many design engineers have been trained?

India set an initial target of training **85,000 design engineers in 10 years**. About **70,000** have been trained in four years.



Talent progress. Bars are drawn roughly to scale.

Who is doing the training?

315 universities train students on complex chip design using the latest EDA tools. Around 68,000 students have already been trained there. In a separate statement, the minister expects 400 engineering colleges and 105 startups to use industry-grade tools.

What about technicians?

The skilling target under ISM 2.0 is **one lakh technicians**. The target may need to be increased.

How many design companies are expected?

The minister expects at least **200 chip design companies** under ISM 2.0. More than 105 design startups already have tools, and 20 secured venture capital.

What happened at SEMICON India 2026?

Day 2 saw **25 MoUs and announcements**.

> **Think it through:** Is the target missed or on track?
>
> Compare the bars. About 70,000 is close to 85,000, and four years is much less than ten.

Quick check 11. True or false: India trained about 70,000 design engineers within four years. *(True or False?)* See answer ↓

Quick check 12. True or false: The ISM 2.0 skilling target is one lakh technicians. *(True or False?)* See answer ↓

Exam Practice

Remember this

- **Semicon 2.0:** Approved July 2026, Rs 1,27,500 crore, six pillars
- **ISM 1.0:** Rs 76,000 crore, 50% fab support, six-year plan met in four
- **Units:** 12 approved, 5 producing, first fab in 2028
- **SiCSem:** Odisha, SiC diodes and MOSFETs, Rs 3,406 crore
- **Talent:** 70,000 design engineers; one lakh technicians targeted

Explain it back: Which pillar comes first in Semicon 2.0, and when is the first fab due?

Practice MCQs

1. Tata Semiconductor Assembly and Test Pvt. Ltd. is located at Jagiroad, in which state?

A. Gujarat

B. Odisha

C. Uttar Pradesh

D. Assam

See answer ↓

2. Which of the following facilities became India's first operational plant under the current India Semiconductor Mission cycle, inaugurated on 28 February 2026?

A. HCL-Foxconn JV plant, Uttar Pradesh

B. Tata Electronics-PSMC fab, Dholera, Gujarat

C. Micron's ATMP plant, Sanand, Gujarat

D. CG Power OSAT plant, Sanand, Gujarat

See answer ↓

3. Under which organisational structure does the India Semiconductor Mission operate?

A. As a public sector undertaking

B. As a regular department within MeitY

C. As a joint venture with private semiconductor companies

D. As an independent business division inside Digital India Corporation

See answer ↓

4. India's first commercial semiconductor fab is being built in Dholera, Gujarat, by Tata Electronics in partnership with which company, and what process node does it target?

A. Micron Technology; 3nm and below

B. Taiwan's PSMC; 28nm and below

C. Intel; 2nm and below

D. Samsung; 14nm and below

See answer ↓

5. Which statement about semiconductor manufacturing is correct?

A. A fab makes chips on wafers, while an OSAT plant assembles and tests finished chips

B. An OSAT plant makes chips on wafers, while a fab only packs them

C. Both terms mean the same kind of plant

D. Neither is covered by the India Semiconductor Mission

See answer ↓

6. SicSem Pvt. Ltd.'s compound-semiconductor fab is located near which city?

A. Bhubaneswar, Odisha

B. Guwahati, Assam

C. Noida, Uttar Pradesh

D. Ahmedabad, Gujarat

See answer ↓

7. When was India Semiconductor Mission (ISM) 1.0 approved, and what was its outlay?

A. August 2021; ₹50,000 crore

B. December 2021; ₹1.27 lakh crore

C. December 2021; ₹76,000 crore

D. January 2022; ₹1 lakh crore

See answer ↓

Answer Key

1. **D.** Tata Semiconductor Assembly and Test is located at Jagiroad, Morigaon district, Assam, on the site of the old Nagaon Paper Mill — a ₹27,000 crore facility.

   ↑ Q1

2. **C.** Micron's assembly-test-packaging (ATMP) plant at Sanand, Gujarat, was inaugurated on 28 February 2026, becoming the first operational facility from this semiconductor mission cycle.

   ↑ Q2

3. **D.** ISM operates as an independent business division inside Digital India Corporation, giving it its own administrative and financial autonomy. ↑ Q3

4. **B.** Tata Electronics has partnered with Taiwan's PSMC to build India's first commercial fab, targeting 28nm-and-below chips, used in cars, industrial controls, and everyday electronics. ↑ Q4

5. **A.** A fab makes the chip. An OSAT plant, such as Micron's at Sanand, assembles, tests and packs it. Both are supported by the India Semiconductor Mission. ↑ Q5

6. **A.** SicSem's compound-semiconductor fab sits at Jatni, near Bhubaneswar, Odisha, a roughly $220 million facility developed with UK-based Clas-SiC Wafer Fab.

   ↑ Q6

7. **C.** ISM 1.0 was approved in December 2021, with an outlay of ₹76,000 crore, offering up to 50% fiscal support to approved projects. ↑ Q7

Quick-check answers

1. **True.** The Cabinet approved it in July 2026. ↑ 1
2. **False.** It rests on six pillars, from design to talent. ↑ 2
3. **True.** It met its objectives in just four years. ↑ 3
4. **False.** The support is 50% of the project cost, on a pari-passu basis. ↑ 4
5. **True.** The cumulative investment is over Rs 1.64 lakh crore. ↑ 5

6. **False.** PIB gives 2028 for the first fab. ↑ 6
7. **True.** The unit also covers 21.889 acres. ↑ 7
8. **True.** The project is also expected to generate about 1,270 jobs. ↑ 8
9. **True.** Production tape-out is targeted for 2027. ↑ 9
10. **True.** The remaining 105 are startups. ↑ 10
11. **True.** The original target was 85,000 in 10 years. ↑ 11
12. **True.** The target may need to be increased. ↑ 12

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